Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A lateral double-diffused metal oxide semiconductor (LDMOS) device comprising:

a gate region;

a body region under the gate region; and

an enhanced drift region under the gate region whereby the enhanced drift region purposely overlaps the body region, and wherein the enhanced drift region and the body region are both self-aligned to the gate region and therefore self-aligned to each other;

~~a drain region within the enhanced drift region such that the enhanced drift region is under the entire drain region; and~~

~~a layer, well, or substrate under the enhanced drift region and the body region, wherein the layer, well, or substrate has the same conductivity type as the enhanced drift region~~.

2. (cancelled)

3. (cancelled)

4. (cancelled)

5. (currently amended) A lateral double-diffused metal oxide semiconductor (LDMOS) device comprising:

a gate region, the gate region including a gate and gate oxide;

a body region under the gate region;

an enhanced drift region under the gate region whereby the enhanced drift region purposely overlaps the body region, and wherein the enhanced drift region and the body region are both self-aligned to the gate region and therefore self-aligned to each other;

a drain region within the enhanced drift region ~~such that the enhanced drift region is under the entire drain region~~; and

a layer, well or substrate under the enhanced drift region and the body region~~,~~ ~~wherein the layer, well or substrate has the same conductivity type as the enhanced drift region~~.

6. (cancelled)

7. (original) The LDMOS device of claim 5 wherein the enhanced drift region purposely overlaps the lateral tail of the body region.

8. – 14. (cancelled)

15. (previously presented) The LDMOS device of claim 1 wherein the enhanced drift region purposely overlaps the lateral tail of the body region.

16. (currently amended) The LDMOS device of claim [1] 24 wherein the conductivity type of the enhanced drift region and the layer, well, or substrate is N-type.

17. (currently amended) The LDMOS device of claim [1] 24 wherein the conductivity

type of the enhanced drift region and the layer, well, or substrate is P-type.

18. (currently amended) The LDMOS device of claim [1] 24 wherein the layer, well, or substrate is an epitaxial layer, and further comprising a buried layer provided under the epitaxial layer and above a substrate, the buried layer having the conductivity type of the epitaxial layer and a different conductivity type than the substrate.

19. (previously presented) The LDMOS device of claim 5 wherein the conductivity type of the enhanced drift region and the layer, well, or substrate is N-type.

20. (previously presented) The LDMOS device of claim 5 wherein the conductivity type of the enhanced drift region and the layer, well, or substrate is P-type.

21. (previously presented) The LDMOS device of claim 5 wherein the layer, well, or substrate is an epitaxial layer, and further comprising a buried layer provided under the epitaxial layer and above a substrate, the buried layer having the conductivity type of the epitaxial layer and a different conductivity type than the substrate.

22. (new) The LDMOS device of claim 1 further comprising a drain region within the enhanced drift region.

23. (new) The LDMOS device of claim 22 wherein the enhanced drift region is under the entire drain region.

24. (new) The LDMOS device of claim 22 further comprising a layer, well, or substrate under the enhanced drift region and the body region, wherein the layer, well, or substrate has the same conductivity type as the enhanced drift region.

25. (new) The LDMOS device of claim 5 wherein the enhanced drift region is under the entire drain region.

26. (new) The LDMOS device of claim 5 wherein the layer, well, or substrate has the same conductivity type as the enhanced drift region.